Remarks

Claims 21, 22 and 25-50 are pending in the application. Claims 1-20 were previously withdrawn per an election made in response to a restriction requirement. Claims 21, 22, 25-33, 41-45 and 48 stand rejected under 35 U.S.C. §102(e) as being anticipated by Pham (U.S. Patent No. 6,803,813). Claims 34-40, 46-47 and 49-50 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pham in view of Figure 2 of Applicant's admitted prior art. Applicant respectfully traverses.

Pham does not teach or suggest all of the recited elements of the pending claims.

Claims 21, 22, 25-33, 41-45 and 48 stand rejected under 35 U.S.C. §102(e) as being anticipated by Pham (U.S. Patent No. 6,803,813). Claims 34-40, 46-47 and 49-50 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pham in view of Figure 2 of the Applicant's specification.

Applicant traverses the rejections. The reference relied upon by the Examiner does not teach or suggest each element of the invention as claimed.

The Examiner asserts that Pham discloses a resistor/capacitor oscillator (102). However, Pham contradicts the Examiner. Pham states that the "**tunable impedance circuit** 102 is an RC circuit" that includes "a tunable resistive circuit 102r ... and a substantially fixed capacitive circuit 102c." Col. 4, line 55 et seq., *emphasis added.* "The terminal voltage V_C across the capacitive circuitry 102c is reset by a shunt switch 102s every half cycle of an **external clock signal** CLK1 having a clock signal frequency f_{CLK1}." Col. 5, line 13 et seq., *emphasis added.* And, finally, "the voltage VC across the capacitive crciutry 102c is **a ramp signal** which will be reset during the time that the clock signal CLK1 is asserted." Col. 5, line 23 et seq., *emphasis added.* Pham appears to clearly describe a circuit for generating a ramp signal in response to an externally supplied clock signal – not an oscillator, as claimed by the Examiner.

It appears that the claimed oscillator is quite clearly absent from the reference relied upon by the Examiner. Therefore, the reference does not anticipate the present invention as set forth in claims 21-22, 25-33, 41-45 and 48. Also, there is no teaching or suggestion for an oscillator in the combination relied upon by the Examiner. Therefore, no prima facie case for obviousness has been established for claims 34-40, 46-47 and 49-50.

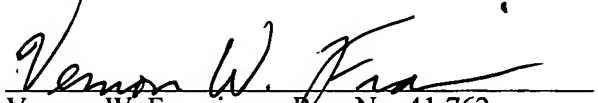
In addition, with regard to claim 26, the Examiner's assertion that Pham shows that the substantially constant current (IR) is mirrored for alternatingly charging and discharging a capacitor 102c of the RC oscillator appears to be contradicted by Pham. Pham teaches that "The terminal voltage V_C across the capacitive circuitry 102c is reset by a shunt switch 102s

every half cycle of an external clock signal CLK1 having a clock signal frequency f_{CLK1}." Col. 5, line 13 et seq. Unlike the invention as claimed in claim 26, the voltage across capacitive circuitry 102c is discharged by the external clock signal closing a switch rather than a mirrored current.

With regard to claims 36-37, Pham appears to contradict the Examiner's assertion that capacitors 116c of Pham are tunable capacitors. Pham states that 102c is a substantially fixed capacitive circuit. Col. 4, lines 55-62. There appears to be no teaching in Pham for tunable capacitors – the symbol for 116c in Figure 3 does not include a diagonal arrow to indicate variability, as do variable resistor circuits 102r and 116r.

The application is considered in good and proper form for allowance, and the Examiner is respectfully requested to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,



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